REMARKS

Applicant thanks the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119, and receipt of a certified copy of the priority document.

Applicant also thanks the Examiner for considering the references cited with the Information Disclosure Statements filed December 24, 2003 and August 17, 2005.

I. Rejection under 35 U.S.C. § 103(a)

Claims 1-3, 5-10, 12-14 and 18-20 have been amended in a non-narrowing manner to correct grammatical and typographical errors unrelated to patentability, therefore no estoppel is indicated.

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Delp et al., U.S. 6,334,174 ("Delp"), in view of Ozawa et al., U.S. 6,483,772 ("Ozawa"), and Solomon et al., U.S. 6,681,293 ("Solomon"). Applicant respectfully traverses this rejection because the references do not teach or suggest at least a read data input circuit having variable input timing for inputting read data output from a memory or a write data output circuit having variable output timing for outputting write data to the memory, as recited by claim 1.

The Examiner asserts that Delp discloses these recitations (col. 7, ll. 5-19). The portion of Delp cited by the Examiner, however, merely discloses a variety of timing characteristics relevant to different types of memory storage devices (col. 7, ll. 5-19). Delp discloses a tuning circuit 22 with a programmable delay counter 24 and a configuration register 26 which combine to insert programmable delays equivalent to a selected number of clock cycles between memory

control operations (col. 7, ll. 19-33, 49-55). Memory control operations are implemented by a plurality of memory specific state machine/support logic blocks configured to implement various timing characteristics and protocols necessary for interfacing with different memory types (col. 10, ll. 45-54). Therefore, Delp discloses different circuit configurations necessary to read and write to different memory types. Delp does not, however, teach or suggest at least the singular read data input circuit or write data output circuit as recited in claim 1.

Ozawa does not cure the deficiencies of Delp. The Examiner alleges that Ozawa discloses a write mask circuit for controlling different write masks (col. 1, ll. 34-36, col. 2, ll. 4-22, and col. 8, ll. 39-47). Ozawa discloses circuitry in a memory device that allows the memory device to be enabled for either the data mask method of masking data or the variable burst length method of masking data by either bonding or not bonding an inner lead to an option pad on the semiconductor chip (Figs. 1, 3 and 10, and col. 5, ll. 1-11). Therefore, Ozawa teaches a mask circuit enabled by hard-wiring, not a circuit for controlling different write masks, as recited in claim 1. Further, the combination of Delp and Ozawa does not disclose at least a read data input circuit having variable input timing or a write data output circuit having variable output timing as recited in by claim 1. Since neither of the references teaches or suggests at least the variable timing input or output circuits of the invention recited in claim 1, Applicant submits that one of ordinary skill in the art would not be motivated to combine the references.

Likewise, the combination of Delp, Ozawa and Solomon does not teach or suggest all elements of claim 1. Solomon is directed to purging data from a processor's fast cache memory (col. 2, ll. 38-46) and discloses a DRAM initialization procedure (col. 27, ll. 39 - col. 28, ll. 14),

but fails to disclose at least the read data input circuit or the write data output circuit, as recited by claim 1. Further, since none of the references suggests at least a read data input circuit having variable input timing or a write data output circuit having variable output timing as recited in by claim 1, Applicant submits that one of ordinary skill in the art would not be motivated to combine the references.

Since the combined references fail to disclose every element of claim 1, Applicant respectfully submits that claim 1 is patentable over Delp in view of Ozawa and Solomon. Additionally, claims 2-10 are patentable over the prior art at least by virtue of their dependency. Applicant respectfully requests that the rejections of claims 1-10 be withdrawn.

Claim 11 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Delp in view of Ozawa and Solomon as applied to claim 1 above, and further in view of Chang, U.S. 6,621,754 ("Chang"). Chang's invention discloses changing the logic level supply voltage available to different DIMM slots based only on the presence of a SDRAM DIMM in a DIMM slot (col. 2, ll. 35 - col. 3, ll. 7). Since the combination of Chang, Delp, Ozawa and Solomon does not teach or suggest at least the read data input circuit or the write data output circuit recited in claim 1, one of ordinary skill in the art would not be motivated to combine the references. Therefore, Applicant respectfully submits that claim 11 is patentable over the prior art.

Claims 12-17 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Delp in view of Ozawa and Solomon as applied to claims 1-3 above, and

further in view of Doyle, U.S. 5,982,655 ("Doyle"). The invention in Doyle allows different types of memory to be connected to a single DIMM socket (col. 2, ll. 9-16). Doyle discloses a set of four discrete buffers on a multi-pin integrated circuit package 50 used to route memory control signals and read/write enable signals from a multiplexer 16 to a memory, and to provide a timing match between the memory and the multiplexer (Fig. 2 and col. 8, ll. 4-8, 47-53). Since the combination of Delp, Ozawa, Solomon and Doyle does not teach or suggest at least a semiconductor memory device comprising a read data input circuit having variable input timing for inputting read data output from said memory, or a write data output circuit having variable output timing for outputting write data to said memory, as recited by claim 1, one of ordinary skill in the art would not be motivated to combine the references. Applicant respectfully submits that claims 12-17 are patentable over the prior art.

Claims 18-20 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Delp in view of Ozawa and Solomon as applied to claims 1-3 above, and further in view of Park et al. ("Park"), U.S. 6,480,409. Park discloses a memory module with a termination resistor. One of ordinary skill in the art would not be motivated to combine Delp, Ozawa, Solomon and Park since the combination does not teach or suggest at least the read data input circuit or the write data output circuit recited in claim 1. Therefore, Applicant respectfully submits that claims 18-20 are patentable over the prior art.

Since combinations of the Delp, Ozawa, Solomon, Chang, Doyle, and Park references do not teach or suggest at least the read data input circuit or the write data output circuit as recited by claim 1, and since one of ordinary skill in the art would not be motivated to combine these

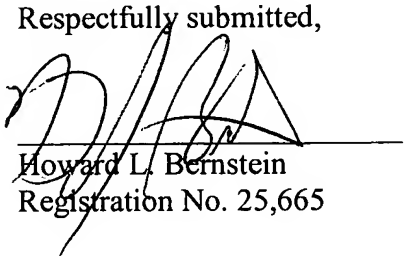
references, Applicant respectfully submits that claim 1 is patentable over these references. Since claims 11-20 depend from claim 1, and claim 1 is patentable over the prior art, Applicant submits that claims 11-20 are patentable over the prior art and respectfully requests withdrawal of the 35 U.S.C. § 103(a) rejections of these claims.

II. Conclusion

In view of the above, Applicant submits that claims 1-20, which are all the claims presently pending in the application, are in condition for allowance. Reconsideration and allowance of this application are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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